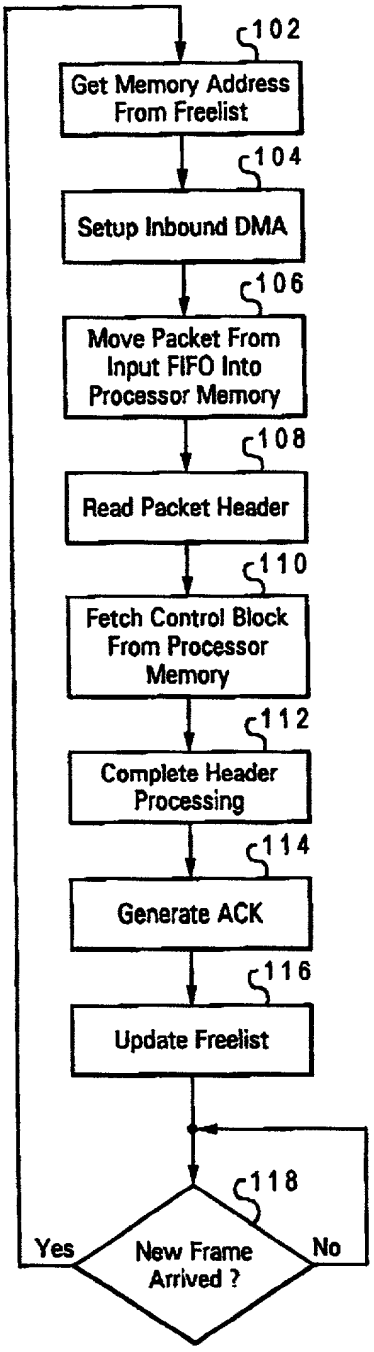

Fig. 1
Prior Art

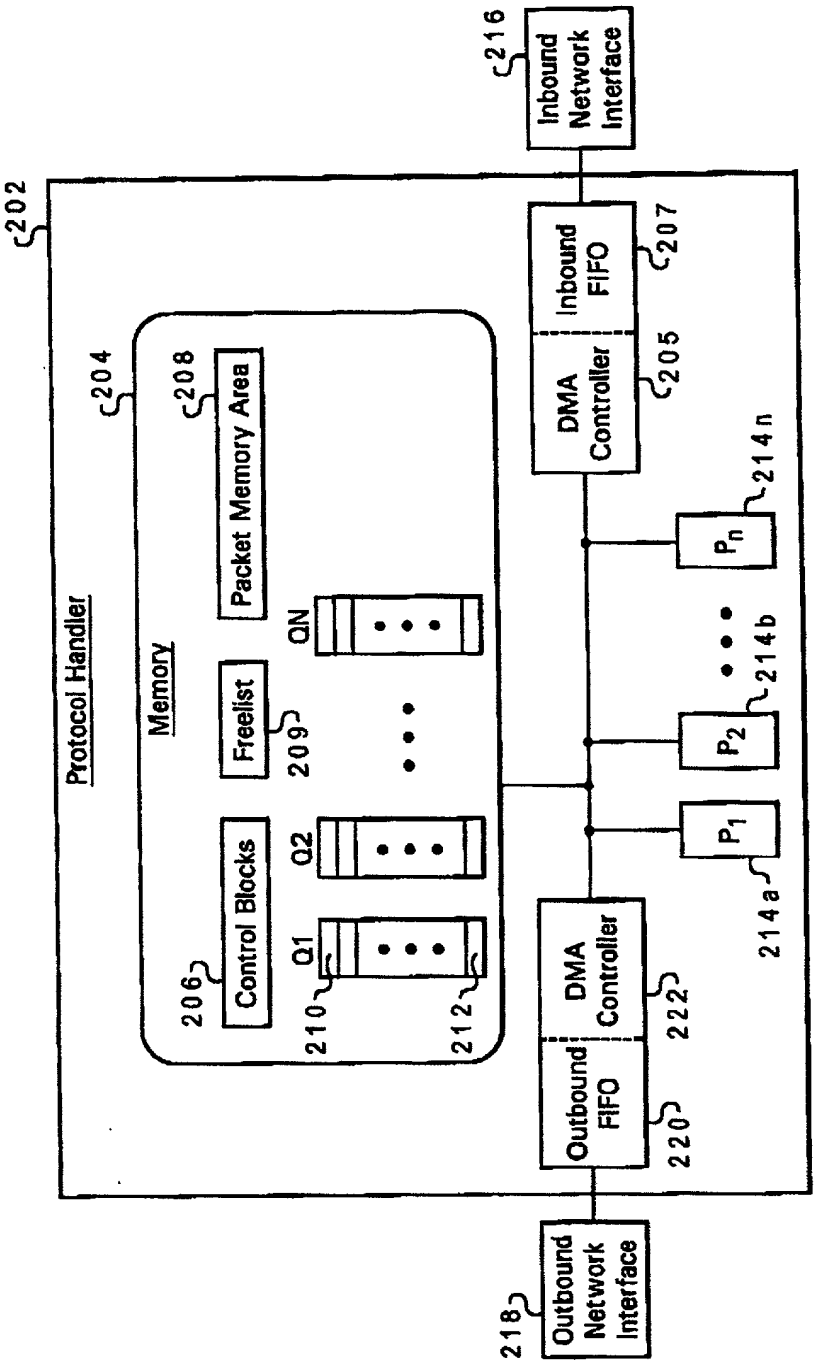
202
Protocol Handler
204
Memory
206
Control Blocks
208
Packet Memory Area
209
Freelist
210
Q1
212
Q2
QN
216
Inbound Network Interface
207
Inbound FIFO
205
DMA Controller
214n
Pn
214b
P2
214a
P1
222
DMA Controller
220
Outbound FIFO
218
Outbound Network Interface

Fig. 2A

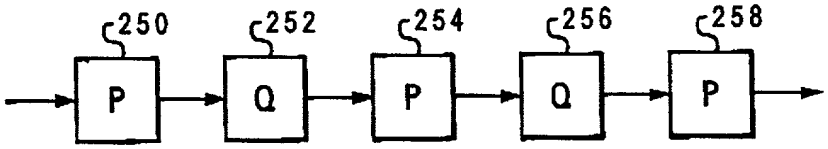

Fig. 2B

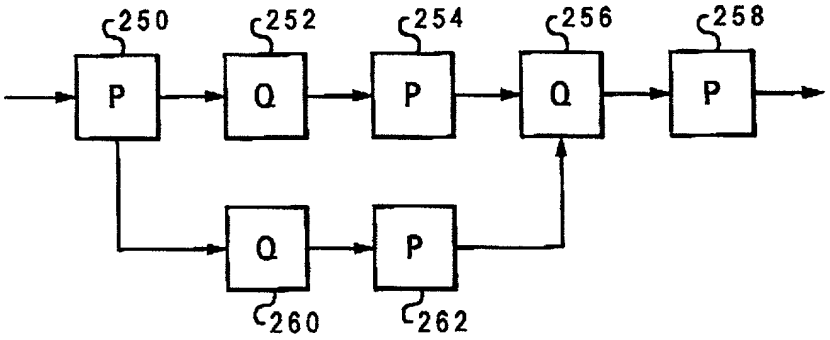

Fig. 2C

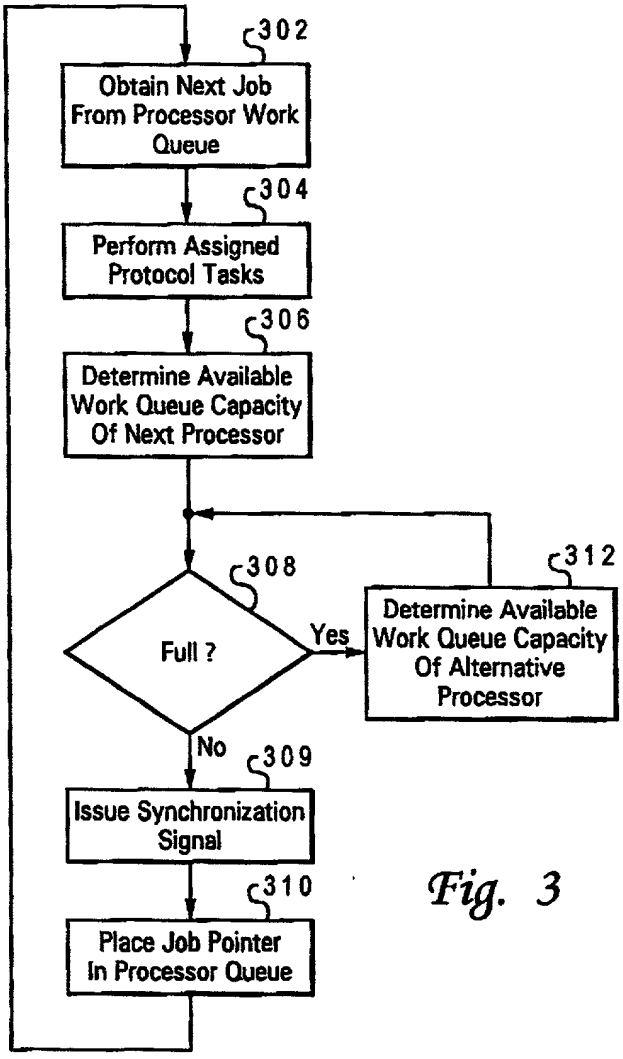
302
Obtain Next Job From Processor Work Queue
304
Perform Assigned Protocol Tasks
306
Determine Available Work Queue Capacity Of Next Processor
308
Full ?
Yes
312
Determine Available Work Queue Capacity Of Alternative Processor
No
309
Issue Synchronization Signal
310
Place Job Pointer In Processor Queue

Fig. 3

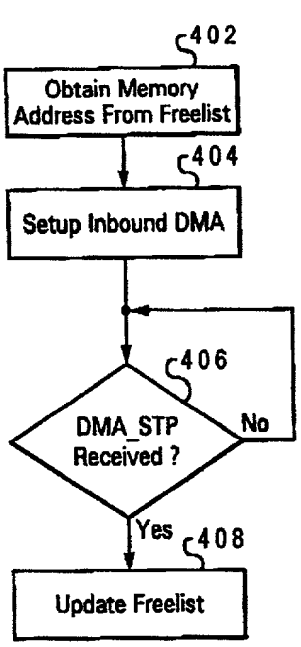
402
Obtain Memory Address From Freelist
404
Setup Inbound DMA
406
DMA_STP Received ?
No
Yes
408
Update Freelist

Fig. 4A

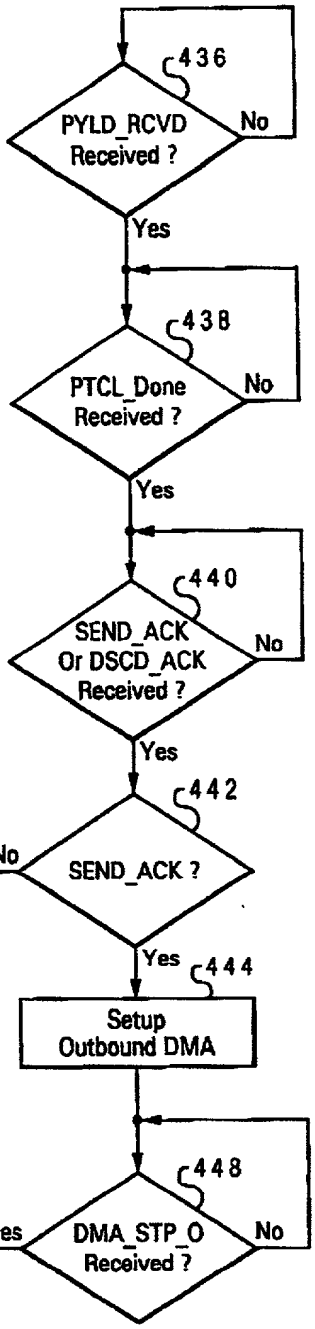
436
PYLD_RCVD Received ?
No
Yes
438
PTCL_Done Received ?
No
Yes
440
SEND_ACK Or DSCD_ACK Received ?
No
Yes
442
SEND_ACK ?
No
Yes
444
Setup Outbound DMA
446
Update Freelist
448
DMA_STP_O Received ?
Yes
No

Fig. 4C

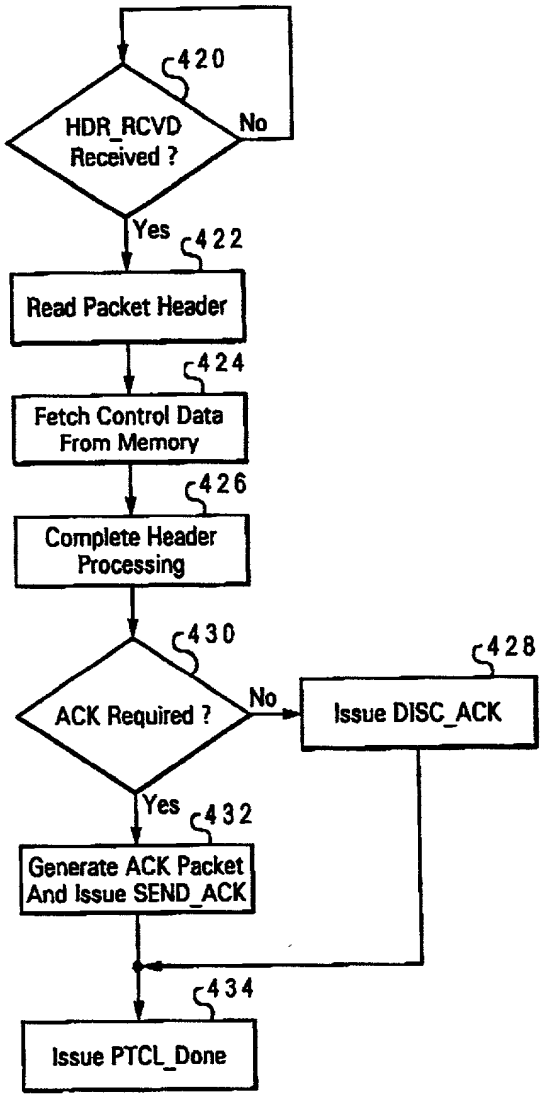
420
HDR_RCVD Received ?
No
Yes
422
Read Packet Header
424
Fetch Control Data From Memory
426
Complete Header Processing
430
ACK Required ?
No
428
Issue DISC_ACK
Yes
432
Generate ACK Packet And Issue SEND_ACK
434
Issue PTCL_Done

Fig. 4B

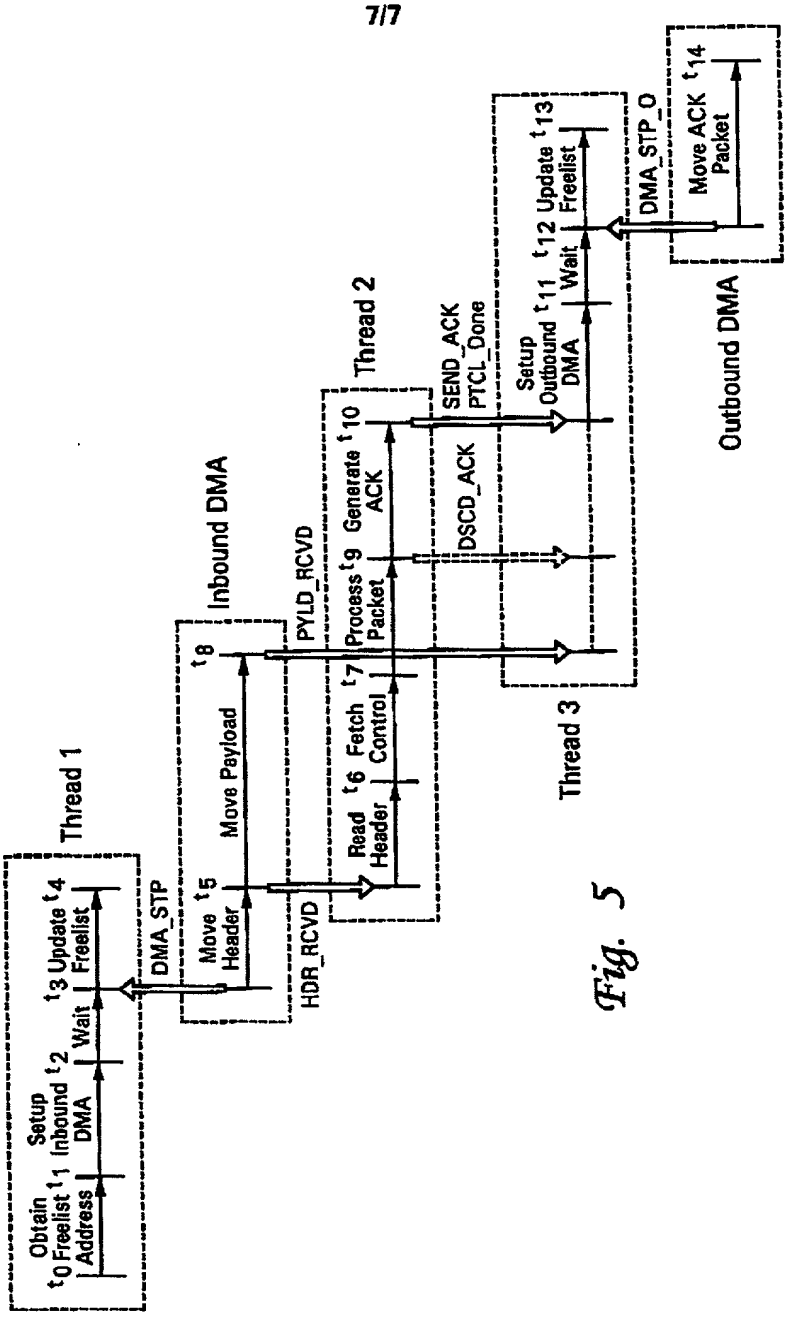
Thread 1
Obtain Freelist Address
t0
t1
Setup Inbound DMA
t2
Wait
t3
Update Freelist
t4
DMA_STP
Inbound DMA
Move Header
t5
HDR_RCVD
Move Payload
t8
PYLD_RCVD
Thread 2
Read Header
t6
Fetch Control
t7
Process Packet
t9
Generate ACK
t10
DSCD_ACK
SEND_ACK
PTCL_Done
Thread 3
Setup Outbound DMA
t11
Wait
t12
Update Freelist
t13
DMA_STP_0
Outbound DMA
Move ACK Packet
t14

Fig. 5